REMARKS

I. Introduction

In response to the Office Action dated July 14, 2009, Applicant has amended claims 5, 9 and 13 in order to further clarify the claimed subject matter. Support for the amendments may be found, for example, in paragraphs [0081] and [0082] of the specification. In addition, Fig. 1(d) has been amended and new Fig. 8 representing the limitation in claim 12 has been added. No new matter has been added.

For the reasons set forth below, Applicant respectfully submits that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claims 5, 7, 13, 16, 18-20, 24 And 25 Under 35 U.S.C. § 102

Claims 5, 7, 13, 16, 18-20, 24 and 25 stand rejected under 35 U.S.C. § 102(b) as being anticipated by En et al. (USP No. 6,548,361); and claims 5 and 18-20 under 35 U.S.C. § 102(e) are rejected as being anticipated by Yu (USP No. 6,893,930). Applicant respectfully traverses these rejections for at least the following reasons.

Features of amended claim 5 include the steps of performing a first heat treatment of the amorphous layer at a prescribed temperature in order to restore a crystal structure of the amorphous layer in a region from the first depth to a second depth. The second depth is shallower than the first depth such that the amorphous layer shrinks to the second depth from the first depth. For example, as is shown in Fig. 1D, the first depth A extends down to the defects layer, whereas the second depth B extends to the amorphous-crystal interface. As such, as shown in Figs. 2A-B, upon heat treatment at a prescribed temperature, the amorphous layer 101 shrinks from the depth A to the depth B.

Another feature of claim 5 is that after the first heat treatment, a first impurity layer is formed of a second conductivity type which has a pn junction at a third depth by introducing ions into the amorphous layer extending from the surface of the semiconductor region to the second depth. The third depth is shallower than the second depth. As is shown in Fig. 1D, the third depth C corresponds with the pn junction 104. In addition, as can be seen in Fig. 2C, the impurities 108 are implanted in the amorphous layer to form a pn junction between the impurity layer 108 and the substrate 100.

In addition, claim 5 recites performing a second heat treatment of the amorphous layer in a region from the surface of the semiconductor region to the second depth using solid phase epitaxy and restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth. For example, as shown in Fig. 3B, a heat treatment restores all the remaining amorphous layer 101 to crystalline form.

In contrast, En merely teaches heat treating the amorphous layer to form a crystal layer. En shows that "the anneal cycle can also used to recrystallize the amorphous area 64" (see, col. 7, lines 56-57). However, En fails to teach "a second depth that is shallower than the first depth" with regard to the semiconductor layer. For example, as is shown in Figs. 3A-D of En, only one layer of amorphous region 64 is converted into crystalline structure 16. In fact, En states that "separate anneal cycle . . . can be carried out" (see, col. 8, lines 1-4 of En), which clearly shows that this step is not necessary. As such, it is clear that En fails to teach or suggest the feature that the recrystallization is carried out to the second depth.

Moreover, as En fails to disclose a second depth, En also fails to disclose a third depth. As such, En fails to teach or suggest performing a second heat treatment of the amorphous layer

in a region from the surface of the semiconductor region to the second depth using solid phase epitaxy and restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth. Nor does En teach a first impurity layer formed of a second conductivity type which has a pn junction at a third depth by introducing ions into the amorphous layer extending from the surface of the semiconductor region to the second depth.

Amended claim 13 recites the features of after the first heat treatment, a first impurity layer is formed of a second conductivity type which has a pn junction at a third depth by introducing ions into the amorphous layer extending from the surface of the semiconductor region to the second depth; and performing a second heat treatment of the amorphous layer in a region from the surface of the semiconductor region to the second depth using solid phase epitaxy and restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth, which are the same as those in claim 5. Accordingly, it is clear that En fails to teach all of the limitations of claims 5 and 13 of the present disclosure.

Turning to Yu '930, Yu fails to disclose or suggest that after the first heat treatment, performing a second heat treatment for restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth. Importantly, Yu is completely silent with regard to a second depth. As is clear in the figures of Yu, the depth of the amorphous layer does not change. Accordingly, Yu also fails to disclose all of the limitations of claim 5 of the present disclosure.

Anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently in a prior art reference, *Akzo N.V. v. U.S. Int'l Trade*

Commission, 808 F.2d 1471 (Fed. Cir. 1986). At a minimum, for the reasons set forth above, En and Yu do not disclose performing a first heat treatment of the amorphous layer at a prescribed temperature, restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth; after the first heat treatment, forming a first impurity layer of a second conductivity type which has a pn junction at a third depth that is shallower than the second depth by introducing ions into the amorphous layer extending from the surface of the semiconductor region to the second depth; and performing a second heat treatment of the amorphous layer in a region from the surface of the semiconductor region to the second depth using solid phase epitaxy and restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth. Therefore, as it is apparent from the foregoing that En and Yu fail to anticipate amended claims 5 and 13 or any dependent claims thereon, Applicant respectfully requests that the § 102 rejection be withdrawn.

III. The Rejection Of Claims 5-7 And 9-25 Under 35 U.S.C. § 103

Claims 6 and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over En et al. (USP No. 6,548,361) in view of Yu et al. (USP No. 6,893,930); claims 6 and 7 as being unpatentable over Yu '930; claim 17 as being unpatentable over En in view of Wu et al. (USP No. 6,391,751); claims 9, 11, 14 and 21-23 as being unpatentable over En in view of Yu (USP No. 6,521,502); claim 10 as being unpatentable over En in view of Yu '502 and further in view of Yu '930; claim 12 as being unpatentable over En in view of Yu '502 and further in view of Wu; claims 5-7, 9-11, 13-16, 18-25 as being unpatentable over Applicant's Admitted Prior Art ("AAPA") in view of En; and claims 12 and 17 as being unpatentable over AAPA in view of En

and further in view of Wu. Applicant respectfully traverses these rejections of the pending claims for at least the following reasons.

As stated above in the arguments for the § 102 arguments, En and Yu '930 fail to disclose the limitations of claims 5 and 13. Furthermore, as amended claim 9 contains the same undisclosed features as claim 5, Applicant submits that En and Yu '930 also fail to disclose the limitations of claim 9 as well for at least the reasons as discussed above.

Moreover, the AAPA fails to remedy this deficiency. The AAPA discloses, as shown in FIG. 6(b), a drain extension 15 is formed by implanting boron ions into the amorphous layer 13 as a dopant at implantation energy of 1 keV or less." See, the specification, paragraph [0009]. Moreover, as shown in FIG. 7(b), heat treatment is conducted for several minutes at a temperature of 500°C to 800°C. As a result, the crystal structure of the amorphous layer 13 is restored, and there is no longer an amorphous region in the silicon substrate 10." See, the specification, paragraph [0012]. Then, boron ions are implanted as a dopant to form the drain extension 15 and are rapidly activated in the amorphous layer 13 without diffusion during restoration of the crystal structure of the amorphous layer 13 to form a shallow pn junction. See, the specification, paragraph [0013].

As such, in the AAPA the "forming a first impurity layer and second impurity layer" would be carried out before the heat treatment for restoring a crystal structure of the amorphous layer. Thus, the AAPA merely teaches restoring a crystal structure of the entire amorphous layer, and fails to disclose or suggest restoring the crystal structure in a region from the surface of the semiconductor region to a second depth. The AAPA says nothing about a second layer or a third layer.

In view of the foregoing, the AAPA fails to teach the features recited in claims 5, 9 and 13 of the present disclosure.

Moreover, Yu '502 does not and is not relied upon to remedy this deficiency.

In order to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. As is clearly shown, En, Yu and the AAPA do not disclose the step of after the first heat treatment for restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth, forming a first impurity layer, performing a second heat treatment for restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth. Accordingly, Applicants submit that En, Yu and the AAPA do not render claims 5, 9 and 13 of the present disclosure obvious and as such, claims 5, 9 and 13 are patentable and allowable over the cited prior art. Accordingly, Applicants respectfully request that the § 103(a) rejections of claims 5, 9 and 13 be withdrawn.

IV. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 5, 9 and 13 are patentable for the reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

V. Conclusion

Having fully responded to all matters raised in the Office Action, Applicant submits that all claims are in condition for allowance, an indication of which is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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